Changes Approved 4/20/05 JJ

AMENDMENTS TO THE SPECIFICATION

Please replace the specification with the attached substitute specification (marked and clean versions). No new matter has been added.

Please replace the paragraph beginning on page 1, line 36, with the following replacement paragraph:

Figure 1 shows the boundary scan principle and the application when testing connection lines on an assembly. The boundary scan input cells BScIN are located between the input pins E1 to En and the core logic CL (for: Core Logic) of a device IC1 (for: Integrated Circuit) and the boundary scan output cells BScOUT are located between the core logic and the output pins A1.1 to An. The BSc cells BScIN and BScOUT form the individual memory cells of the shift register. The shift register can be loaded in series via the input TDI (test data in) or in parallel via the input pins E1 to En. Similarly, the output data can be taken in series at the output TDO (test data out) or in parallel at the outputs A1.1 to An. The testing of the connections between the outputs A1~~.1~~ to An of IC1 and the inputs E1 to En of device IC2 is shown in figure 1 as an example. For this purpose, a test bit pattern is pushed in series into the shift register via the input TDI of IC1, until it appears at the BSc output cells BScOUT of IC1. It is then transferred as a parallel bit pattern to IC2, transferred by the BSc input cells BScIN and pushed out in series via the shift register of IC2 at the output TDO, and then analyzed by the test system. The core logic is logically separated from the BSc register during this test.

Please replace the paragraph beginning on page 10, line 5, with the following replacement paragraph:

Figure 8 shows another embodiment of the present invention~~ with terminating resistors outside the device~~.

Please replace the paragraph beginning on page 14, line 11, with the following replacement paragraph:

An exemplary embodiment of the supplementary circuit according to the invention for the LVDS case is shown in figure 9. At the inputs E1~~.1~~ and E1~~.2~~ there are the terminating resistors RT1

and RT2, the other terminals of which are interconnected and connected via pin C to the external 1.2 V voltage source. The comparator K1 is the LVDS input comparator. The comparators K2 and K3, the transistors M1 to M5 and the current source IREF form the exemplary circuit for the boundary scan case. Furthermore, there are two boundary scan cells BSc-Z1 and BSc-Z2, which belong to the normal boundary scan register. In the boundary scan case, the current is mirrored via the transistor M1 onto M2 and M4 from the current source IREF, which generates a reference current. M1, M2 and M4 form a current mirror. The mode of operation of a current mirror and the generation of a reference current are explained variously in the literature, for example /3/ "Paul R. Gray, Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley & Sons, New York, 1984". The current flow through M2 and M4 is intended to be about 1.5 mA in each case, so that a voltage drop of about 75 mV respectively occurs at RT1 and RT2 (1.5 mA * 50 Ω = 75 mV). This can be achieved by the size of IREF and corresponding dimensioning of M1, M2 and M4. In another embodiment, the auxiliary voltages at RT1 and RT2 are generated by current sources IH1 and IH2 which pull a current from the terminal C to GND, as already represented in principle in figure 8.

Please replace the paragraph beginning on page 15, line 32, with the following replacement paragraph:

If the terminating resistors are located outside the device, the current sources with M2 to M5 prevent the inputs of the comparators K2 and K3, which are connected to E1.1 and E1.2, respectively, from floating if there is an interruption between the external terminating resistor and the input circuit, for example because of a pin E1.1 or E1.2 that is not soldered on. If it is necessary that, when there is an interruption of both lines, comparator K1 also emits a defined level to the core logic, it can be detected by an additional monitoring circuit that both inputs are at negative or positive supply voltage - depending on the polarity of the current sources - and, as a consequence, that a defined level is passed on. This corresponds to the prior art and is not explained any further.